What is claimed is:

1. A clock skew indicating apparatus comprising:

a detection circuit for receiving as input first and second clocks and generating as output a compare signal; and

a sampling circuit, according to said compare signal, for asserting an output signal indicative of skew existing between said first and said second clocks.

2. The apparatus as recited in claim 1 wherein said first clock is transmitted with a differential signaling scheme.

3. The apparatus as recited in claim 2 further comprising a first differential-to-single-ended converter receiving said first clock, for providing said detection circuit with a version of said first clock converted into a single-ended signaling scheme.

4. The apparatus as recited in claim 3 wherein said second clock is transmitted with the differential signaling scheme.

5. The apparatus as recited in claim 4 further comprising a second differential-to-single-ended converter receiving said second clock, for providing said detection circuit with a version of said second clock converted into the single-ended signaling scheme.

6. The apparatus as recited in claim 1 wherein the width of said compare signal generated by said detection circuit is substantially proportional to an amount of said skew between said first and said second clocks.

7. The apparatus as recited in claim 6 wherein said sampling circuit samples said compare signal at a predetermined frequency such that said output signal is set to indicate the amount of said skew between said first and said second clocks.

8. The apparatus as recited in claim 7 further comprising a phase-locked loop for providing said sampling circuit with a reference clock running at said predetermined frequency.

9. An apparatus for indicating clock skew within integrated circuits (ICs) of a system, comprising:

a first IC chip operating on a first clock and providing as output said first clock; and

a second IC chip operating on a second clock, comprising:

a detection circuit for receiving as input said first and said second clocks and generating as output a compare signal; and

a sampling circuit, according to said compare signal, for asserting an output signal indicative of skew existing between said first and said second clocks;

wherein the width of said compare signal is substantially proportional to an amount of said skew between said first and said second clocks.

10. The apparatus as recited in claim 9 wherein said first IC chip comprises:

a control pin receiving an enable signal external to said first IC chip; and

an output buffer coupled to receive said first clock, for outputting said first clock under control of said enable signal.

11. The apparatus as recited in claim 9 wherein said first clock is transmitted with a differential signaling scheme.

12. The apparatus as recited in claim 11 wherein said second IC chip comprises a first differential-to-single-ended converter receiving said first clock, for providing said detection circuit with a version of said first clock converted into a single-ended signaling scheme.

13. The apparatus as recited in claim 12 wherein said second clock is transmitted with the differential signaling scheme.

14. The apparatus as recited in claim 13 wherein said second IC chip further comprises a second differential-to-single-ended converter receiving said second clock, for providing said detection circuit with a version of said

second clock converted into the single-ended signaling scheme.

15. The apparatus as recited in claim 9 wherein said sampling circuit samples said compare signal at a predetermined frequency such that said output signal is set to indicate the amount of said skew between said first and said second clocks.

16. The apparatus as recited in claim 15 wherein said second IC chip comprises a phase-locked loop for providing said sampling circuit with a reference clock running at said predetermined frequency.